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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/774,700 | 02/10/2004 | Shunpei Yamazaki | 12732-211001 / US6966 | 8592 |

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| EXAMINER | |
|---|---|
| TRAN, MAI HUONG C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/774,700 | YAMAZAKI ET AL. | |
| | Examiner | Art Unit | |
| | Mai-Huong Tran | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7,9,14 and 27-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,14 and 27-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/17/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

# DETAILED ACTION

## Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 9, 14, 27-71 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Pub. No. 2003/0231263.

Claims 1-7, 9, 14 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication No. 2003/0231263 to Kato et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention by another," or by an appropriate showing under 37 CFR 1.131.

Regarding to claim 1, Kato discloses a semiconductor device comprising a substrate 400; a pixel portion 401 over the substrate 400; a driving circuit 402, 403, 404 over the substrate and having at least one first terminal (fig. 6D); and an integrated circuit 415, 414, 413 having at least one second terminal (fig. 6D) and at least partially overlapped with the driving circuit 402, 403, 404 wherein the first terminal and the second terminal face each others and are electrically connected via a conductive material 508 (page 4, [0076]-0082], and figs. 1A-1C, 6D, 22A).

Regarding to claims 2, 28, 37, 46, 55, 64, the semiconductor device wherein the integrated circuit includes any one of a display controller, a frame memory, a power source circuit, a CPU and a memory (page 6, [0104], [0109], page 14, [0223]).

Regarding to claims 3, 29, 38, 47, 56, 65, the semiconductor device wherein the pixel portion includes any one of a light-emitting element and a liquid crystal element (page 5, [0093]).

Regarding to claims 4, 30, 39, 48, 57, 66, the semiconductor device, wherein the pixel portion includes a light-emitting element having a first electrode, an electroluminescent layer and a second electrode, and wherein the first electrode and the second electrode are translucent (page 4, [0084]).

Regarding to claims 5, 31, 49, 58, 67, the semiconductor device, wherein the semiconductor device is any one of an active matrix type semiconductor device and a passive matrix type semiconductor device (page 4, [0076]).

Regarding to claims 6, 32, 41, 50, 59, 68, an electronic device comprising the semiconductor device wherein the electronic device is any one of a group comprising a display device, a notebook type personal computer, a mobile computer, a player with a recording medium, an electronic book, a video camera, a portable telephone, a digital camera, a head-mount display, a car navigation system, a projector and a car stereo (figs. 21A-21G).

Regarding to claims 7, 33, 42, 51, 60, 69, the semiconductor device wherein the integrated circuit is formed by transcribing an element formation layer formed over a second substrate 406 (page 4, [0076-0078]).

Regarding to claims 9, 34, 43, 52, 70, the semiconductor device, wherein the integrated circuit is formed by laminating the integrated circuit in one layer or two or more layers (figs. 1B-1C).

Regarding to claims 14, 35, 44, 53, 62, 71, the semiconductor device wherein the integrated circuit is electrically connected to part or an entirety of the pixel portion and the driving circuit (page 4, [0076-[0082], and figs. 1A-1C).

Regarding to claim 27, Kato discloses a semiconductor device comprising a substrate 400; a pixel portion 401 over the substrate, a driving circuit 402, 403, 404 over the substrate; and an integrated circuit 413, 414, 415 at least partially overlapped with the driving circuit, with an adhesive layer therebetween (page 10, [0151], figs. 1A-1C, 6D).

Regarding to claim 36, a semiconductor device comprising a substrate; a pixel portion over the substrate, a driving circuit over the substrate; a first integrated circuit at least partially overlapped with the driving circuit; and a second integrated circuit at least partially overlapped with the first integrated circuit (fig. 6D).

Regarding to claim 45, a semiconductor device comprising a substrate, a pixel portion over the substrate, a driving circuit over the substrate, having at least one first terminal; and an integrated circuit having at least one second terminal and at least partially overlapped with the driving circuit, with an adhesive layer therebetween, wherein the first terminal and the second terminal face each other, and are electrically connected via a conductive material 508 (page 4, [0076]-0082], page 10, [0151], and figs. 1A-1C, 6D, 22A).

Regarding to claim 54, Kato discloses a semiconductor device comprising a substrate; a pixel portion over the substrate, a driving circuit over the substrate, a first integrated circuit at least partially overlapped with the driving circuit, with a first adhesive layer therebetween; and a second integrated circuit at least partially overlapped with the first integrated circuit, with a second adhesive layer therebetween (page 4, [0076]-0082], page 10, [0151], and figs. 1A-1C, 6D).

Regarding to claim 63, Kato discloses a semiconductor device comprising a substrate, a pixel portion over the substrate; a driving circuit over the substrate, having at least one first terminal; a first integrated circuit having at least one second tenninal and at least one third terminal, and at least partially overlapped with the driving circuit, with a first adhesive layer therebetween; and a second integrated circuit having at least one fourth terminal and at least partially overlapped with the first integrated circuit, with a second adhesive layer therebetween, wherein the first terminal and the second terminal face each other, and are electrically connected via a first conductive material 508, and wherein the third terminal and the fourth terminal face each other, and are electrically connected via a second conductive material (page 4, [0076]-0082], page 10, [0151], and figs. 1A-1C, 6D, 22A).

## Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MHT

Mai-Huong Tran